	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L10	1112	716/18.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2006/10/04 15:44
2	BRS	L11	1075	703/14.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	2006/10/04 15:45

	Type	Ref #	Hits	Search Text
1	BRS	S466	3368	(national-semiconductor-corporation).as.
2	BRS	S468	10	(national-semiconductor-corporation).as. and (hdl) and (tim$3)
3	BRS	S467	10	(national-semiconductor-corporation).as. and (hdl)
4	BRS	S469	713	(netlist same synthesiz$3) and (hdl) and (tim$3)
5	BRS	S470	81	(netlist same synthesiz$3) and (timing same violat$3)
6	BRS	S472	286	703/19.ccls.
7	BRS	S471	50	(netlist same synthesiz$3) and (timing same violat$3) and HDL
8	BRS	S473	1516	716/6.ccls.

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ignore simulation HDL "timing violations" Search

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H Bhatnagar
E Cerny
R Aitken
M Lindgren
W Chen

[PS] VirtexDS: A Virtex Device Simulator - group of 4 »
S McMillan, B Blodget, S Guccione - at SPIE, 2000 - tpoint.net
... This essentially produces a functional **simulator** which can **ignore** signal glitches and intermediate ... 11. S. Yalamanchili, VHDL: From **Simulation** to Synthesis ...
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Scott P. McMillan, Brandon J. Blodget, and Steven A. Guccione Xilinx Inc., 2100 Logic Drive, San ... - group of 3 »
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... This essentially produces a functional **simulator** which can **ignore** signal glitches and intermediate ... 11. S. Yalamanchili, VHDL: From **Simulation** to Synthesis ...
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Extracting gate-level networks from **simulation** tables - group of 5 »
P Wohl, J Waicukauski - Test Conference, 1998. Proceedings. International, 1998 - doi.ieeecs.org
... Verilog or VITAL tables in VHDL [1], [2 ... equivalent" structural model, engineers **ignore** certain functionality ... intended only for some **simulation** checking (such ...
Cited by 3 - Related Articles - Web Search

DA STANDARDS ACTIVITIES - group of 2 »
PM Hefferan - ACM SIGDA Newsletter, 1988 - portal.acm.org
... applied or in misuse of VHDL's generic parameters ... for example to indicate **timing violations** under certain ... under those conditions and **simulation** processing shall ...
Cited by 1 - Related Articles - Web Search

Example AMBA™ SYstem - group of 2 »
U Guide - rtds.cs.tamu.edu
... The system hierarchy is the structure present in an **HDL simulation** of the EASY system, with the TBTic or TBEasy test bench at the top, and all other modules ...
Related Articles - Web Search

[BOOK] Gate-level Timing Verification Using Waveform Narrowing - group of 5 »
E Cerny - 1994 - sigda.org
... sets of all possible transitions and **ignore** correlation due to ... the algorithm in the hardware description language VHDL and used the **simulator** to perform ...
Cited by 6 - Related Articles - View as HTML - Web Search - Library Search

[BOOK] Advanced Asic Chip Synthesis: Using Synopsys Design Compiler Physical Compiler and Primetime
H Bhatnagar - 2002 - books.google.com
... In addition, the **HDL** coding styles is covered ... those designers who prefer dynamic **simulation** method to ... in debugging the design for possible **timing violations**. ...
Cited by 36 - Related Articles - Web Search - Library Search

Gate-level timing verification using waveform narrowing
J Zejda, E Cerny - Proceedings of the conference on European design automation, 1994 - portal.acm.org

... sets of all possible transitions and **ignore** correlation due ... port using the g function with the VHDL delta delay ... is possible), the next real **simulation** time is ...
Cited by 3 - Related Articles - Web Search

AUTOMATED EXPLORATION OF THE ASIC DESIGN SPACE FOR MINIMUM POWER-DELAY-AREA PRODUCT AT THE REGISTER ... - group of 3 »
F Karakaya - microsys6.engr.utk.edu
... guage (**HDL**) such as VHDL or Verilog at either the behavioral level or at the ... 2. Mapping the **HDL** to a specific process to generate a process-dependent net-list. ...
Related Articles - View as HTML - Web Search

Towards the complete elimination of gate/switch level simulations - group of 3 »
N Krishnamurthy, J Bhadra, MS Abadir, JA Abraham - VLSI Design, 2004. Proceedings. 17th International ..., 2004 - ieeexplore.ieee.org
... conditions of setup and hold **timing violations**, a latch ... environment would not invalidate the **simulation** pattern ... level model allows us to **ignore** the propagation ...
Cited by 2 - Related Articles - Web Search

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Result Page: 1 2 3 **Next**

Google Scholar BETA

"timing violation controller" Search

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Tip: Try removing quotes from your search to get more results.

Your search - **"timing violation controller"** - did not match any articles.

Suggestions:

- Make sure all words are spelled correctly.
- Try different keywords.
- Try more general keywords.
- Try your query on the entire web.

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Web Results **1** - **1** of **1** for **"timing violation controller"**. (**0.28** seconds)

Tip: Try removing quotes from your search to get more results.

NanDigits: whats new
Tune up in **timing violation controller**. Apr 04, 2006. V2.100 released. Per a lot of users' request, add line index in RTL viewer. RTL viewer color control. ...
nandigits.com/whats_new.htm - 10k - Supplemental Result - Cached - Similar pages

Nothing Found

Your search for **"timing violation controller"** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

```
sales offices
```

You can also enter a full question or concept in plain language.

```
Where are the sales offices?
```

- Capitalize proper nouns to search for specific people, places, or products.

```
John Colter, Netscape Navigator
```

- Enclose a phrase in double quotes to search for that exact phrase.

```
"museum of natural history" "museum of modern art"
```

- Narrow your searches by using a + if a search term must appear on a page.

```
museum +art
```

- Exclude pages by using a - if a search term must not appear on a page.

```
museum -Paris
```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Interference

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	176	(timing adj violations)	US-PGPUB	2006/10/04 15:09
2	BRS	L2	1	(timing adj violations) same ignore	US-PGPUB	2006/10/04 15:10
3	BRS	L3	4	(timing adj violations) same HDL	US-PGPUB	2006/10/04 15:10
4	BRS	L4	14	timing same violation same controller	US-PGPUB	2006/10/04 15:11
5	BRS	L5	97	(timing same simulation same HDL)	US-PGPUB	2006/10/04 15:12
6	BRS	L6	9	(timing same simulation same HDL same IC)	US-PGPUB	2006/10/04 15:13
7	BRS	L7	545	(circuit same netlist same simulation)	USPAT	2006/10/04 15:13
8	BRS	L8	53	(circuit same netlist same simulation same ic)	USPAT	2006/10/04 15:15
9	BRS	L9	19	(circuit same netlist same simulation same modules)	USPAT	2006/10/04 15:15

TS